REMARKS

No claims are amended, canceled, or added. Claims 1-22 remain in the Application. Reconsideration of the pending claims is respectfully requested in view of the above amendment and the following remarks.

I. Claims Rejected Under 35 U.S.C. § 103(a)

A. Claims 1-11, 13, 14 and 16-22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Application No. US005150312A issued to Beitel ("Beitel") in view of U.S. Patent Application No. US005519825A issued to Naughton ("Naughton"), and further in view of U.S. Patent No. US006108015A issued to Cross ("Cross"). Applicant respectfully traverses the rejection.

To establish a *prima facie* case of obviousness, the relied upon references must teach or suggest every limitation of the claim such that the invention as a whole would have been obvious at the time the invention was made to one skilled in the art.

Claim 1 recites an apparatus comprising:

> "a display controller;
> an internal frame buffer coupled to the display controller; and
> a control circuitry to copy display data from an external frame buffer to the internal frame buffer, wherein the display data copied into the internal frame buffer is the same display data read by the display controller from the external frame buffer."

Applicant submits that the cited references, separately or combined, do not teach or suggest each of the elements of Claim 1.

Beitel discloses a system that displays an animated sequence of images. The system comprises a display screen 10, a display memory 1, a CPU 2, a main memory 4, and a mass storage device 5 (FIG. 1). Display memory 1 is coupled between CPU 2 and display screen 10. Display memory 1 stores individual pixels of display screen 10 (col. 2, lines 37-39). Stored data in display memory 1 is read out and displayed on display screen 10 in a conventional manner (col. 2, lines 34-36).

To generate animated images on display screen 10, Beitel discloses that a portion of display memory 1 (the present region) is copied into a buffer A in main memory 4. The content

of buffer A is subsequently copied into a buffer B which is also in main memory 4 (FIG. 2c and FIG. 3, blocks 14 and 20).

The Examiner analogizes display memory 1 as the claimed external frame buffer, and buffer B as the claimed internal frame buffer. Although it is recognized that Beitel does not disclose that buffer B is a frame buffer, the Examiner relies on Naughton to supply the teaching of using frame buffers for displaying animated images. The Examiner indicates that a person of ordinary skill in the art would modify the device of Beitel with the teaching of Naughton to replace buffer B by a frame buffer.

Even assuming, for the sake of argument, that a person of ordinary skill in the art would replace both display memory 1 and buffer B by frame buffers, there is nothing in the cited references that teach or suggest that display memory 1 is the external frame buffer and buffer B is the internal frame buffer, as indicated by the Examiner.

Applicant defines the terms "external" and "internal" in the specification at paragraph 10:

> "In one context, the terms "internal memory array" and "internal frame buffer" are used interchangeably to describe a memory space for buffering display data, which resides in the same chip that contains the display controller. Similarly, the terms "external memory array" and "external frame buffer" are used interchangeably to describe a memory space for buffering display data, which resides in a chip separate from the display controller." (Emphasis added).

Cross discloses a display controller that controls an external frame buffer and an internal frame buffer. The Examiner relies on Cross to cure the deficiency of Beitel and Naughton, because "Cross suggests that an on-chip memory provides the controller with fast access storage, and the off-chip memory allows the controller to interface with a memory which may be substantially larger than that which can be provided on-chip." (Office Action at page 5). The Examiner seems to indicate that, because the size of display memory 1 is larger than the size of buffer B, display memory 1 should be characterized as the external frame buffer and buffer B should be characterized as the internal frame buffer. Applicant respectfully disagrees.

Assuming solely for the sake of argument that a person of skill in the art would combine the teaching of the cited references to modify the devices of Beitel (which Applicant continues to contend one would not), the combination would at most produce a system in which display memory 1 is the internal frame buffer and buffer B is the external frame buffer. A skilled person in the art would use display memory 1 as an internal frame buffer exactly because display

memory 1 is larger than buffer B. An example of an internal frame buffer, as disclosed by Cross, may be implemented by a pair of 256Kx16 DRAMs which may provide a display refresh rate of 80 to 100 megabytes/second. Thus, according to the teaching of Cross, an internal frame buffer is typically large enough to accommodate display memory 1. Thus, there is no reason to store only a portion of display memory 1 (e.g., the present region of buffer B) in the faster, more power-efficient internal frame buffer. A skilled person would store as much display data as practically feasible into an internal frame buffer before storing the rest of the data into a larger but slower external frame buffer. Thus, applying the teaching of the cited references, display memory 1 would reside on-chip (i.e., internally) because the size of the display memory fits into the chip, and buffer B (storing a portion of the display memory contents) would reside off-chip (i.e., externally). Thus, the combination of the references would at most teach or suggest copying display data from an internal frame buffer to an external frame buffer, contrary to what the Examiner indicates and what is claimed.

Thus, the cited references, separately or combined, do not teach or suggest the claimed control circuitry "to copy display data from an external frame buffer to the internal frame buffer, wherein the display data copied into the internal frame buffer is the same display data read by the display controller from the external frame buffer."

Analogous discussions apply to independent Claims 9 and 16. Claims 2-8, 10-11, 13-14, and 17-22 respectively depend from Claims 1, 9, and 16 and incorporate the limitations thereof. Thus, for at least the foregoing reasons, Beitel in view of Naughton and further in view of Cross does not teach or suggest these dependent claims.

Accordingly, reconsideration and withdrawal of the rejection of Claims 1-11, 13, 14 and 16-22 are requested.

B. Claims 9-12 and 15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Beitel in view of Naughton and further in view of U.S. Pre-Grant Patent Application No. 2004/10150647A1 applied for by Aleksic et al. ("Aleksic").

Claims 10-12 and 15 depend from Claim 9 and incorporate the limitations thereof. Thus, for at least the foregoing reasons, Beitel in view of Naughton and further in view of Cross does not teach or suggest these dependent claims.

The Examiner relies on Aleksic for disclosing a graphics chip containing a display controller, an internal memory array, and control circuitry. However, Aleksic does not cure the deficiency of the other cited references for failing to teach or suggest that display memory 1 is the claimed internal frame buffer and buffer B is the claimed external frame buffer. Aleksic does not even mention any external frame buffer in the entire disclosure. Thus, Aleksic cannot possibly teach or suggest copying display data from an external frame buffer to the internal frame buffer.

Thus, the cited references, separately or combined, do not teach or suggest the claimed control circuitry "to copy display data from an external frame buffer to the internal frame buffer, wherein the display data copied into the internal frame buffer is the same display data read by the display controller from the external frame buffer."

Accordingly, reconsideration and withdrawal of the rejection of Claims 9-12 and 15 are requested.

CONCLUSION

In view of the foregoing, it is believed that all claims now are now in condition for allowance and such action is earnestly solicited at the earliest possible date. If there are any additional fees due in connection with the filing of this response, please charge those fees to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 4/24/06

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I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Suzanne Johnston 4/24/06

Date